REMARKS

This Amendment and Response is filed in reply to the Final Office Action dated May 21, 2003. The issues presented in the May 21, 2003 Final Office Action are addressed below.

The Examiner objected to the drawings under 37 C.F.R. 1.83(a), indicating the drawings must show every feature of the invention specified in the claims. The objection is traversed. Figs. 1, 2 and 3B are amended to conform to the specification and to more clearly show the features of the invention. In particular, Fig. 1 has been amended to show the connections between the decoupling capacitors 14 and the devices 20. Fig. 2 has been amended to more clearly show the power plane 31 and pads 26, in keeping with the original drawings filed in the case. Fig. 3B has been amended to correctly label the base 48 and correctly identify the power plane 52. As provided below, the Examiner has indicated the amended drawings appear satisfactory. Thus, a formal set of drawings is being submitted with this response. Please note that in the formal drawings submitted herewith, Figs. 1 and 2 have been shown on separate drawing sheets and the drawings sheets have been renumbered accordingly.

In the present response, the drawings and claims 12 and 32 have been amended. Claim 33 has been cancelled without prejudice. The amendments, however, should not be construed in any way as acquiescence to any of the rejections, but rather made solely to expedite prosecution of the instant application. Applicants reserve the option to further prosecute the same or a similar subject matter in the instant or a subsequent application. Applicants' silence with regard to any of the Examiner's rejections should not be construed as acquiescence to any of the rejections. Upon entry of these amendments, claims 12, 21, 22 and 24-32 constitute the claims pending in the present application. Applicants request reconsideration in view of the foregoing changes and the following remarks.

Applicants wish to thank the Examiner for his review of proposed amendments faxed to the Examiner on June 25, July 2, and July 8, 2003 and for the Examiner's subsequent telephonic discussions of the proposed amendments. In the telephonic discussion of July 15, 2003, the examiner indicated the proposed amendment to claim 12, together with the amended drawings appear to overcome the rejection of claim 12 under 35 U.S.C. § 102(b) as being anticipated by Takashi et al. (JP 406, 295, 981A). The amended drawings and claims provided herein reflect those faxed to the Examiner on July 8, 2003. In the telephonic discussion of July 15, 2003, the

Examiner indicated the proposed drawing amendments submitted to the Examiner appeared satisfactory. Applicants appreciate the Examiner's time in reviewing the proposed drawing and claim amendments and discussing the amendments with Applicants.

In the Office Action of May 21, 2003, the Examiner objected to claim 32, contending the decoupling capacitor is electrically connected with only one circuit device. The objection is traversed. Claim 32 has been amended to indicate that the device includes a plurality of decoupling capacitors, as indicated in the figures and described throughout the specification, e.g., see description on page 8 with respect to Fig. 1. Claim 32 further recites that each of said plurality of circuit devices is in electrical communication with at least one of said decoupling capacitors, as shown in Fig. 1.

The Examiner rejected claim 22 as containing subject matter not described in the specification in such a way to enable one skilled in the art to make or use the invention. The rejection is traversed. The amendment to Fig. 2 clarifies the connections between the respective power planes 28, 31 of the decoupling capacitor 14 and the interconnecting layer 16, and between the respective ground planes 29, 33 of the decoupling capacitor 14 and the interconnecting layer 16. Claim 22 recites the structure corresponding to Fig. 2 and reconsideration of the rejection is respectfully requested.

The Examiner rejected claims 12, 21, 25, 30 and 32-33 under 35 U.S.C. § 102(b) as being anticipated by Takashi et al. (JP 406, 295, 981A). The Examiner rejected claims 24, 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. (JP 406,295,981A) in view of Tuckerman (U.S. Patent No. 5,274,270). The Examiner rejected claims 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. in view of Smith (U.S. Patent No. 4,890,192) and rejected claim 31 under 35 U.S.C. § 103(a) as being unpatentable over Takashi et al. in view of Eichelberger (U.S. Patent No. 5,841,193).

Applicants traverse the Examiner's rejections and respectfully requests reconsideration in view of the amendments and remarks.

With respect to the rejections under 35 U.S.C. § 102(b), Takashi et al. describe a semiconductor device, wherein a PN junction protective diode is formed between the N-type diffusion layer 22 and the P-type Si wafer substrate 16 to protect a decoupling capacitor 24 within the device. The P-type Si wafer substrate is an active component of the semiconductor

device, in that the diode is formed between the diffusion layer 22 and the substrate 16. In addition, the decoupling capacitor 24 is formed as part of the interconnecting layer 17 and is coupled to the diffusion layer 22, as indicated by connection 27. In contrast, Applicants provide a device for interconnecting a *plurality of circuit devices*. An interconnect layer having a pattern of circuit connections is formed over discrete decoupling capacitors thereby embedding electrical connections to the decoupling capacitors within the interconnect layer. Circuit devices, such as the Takashi et al. semiconductor device, can be mounted to the surface of the interconnect layer and coupled to the decoupling capacitors through the circuit connections of the interconnect layer. The support base 12 simply provides a mounting surface for Applicants' device and is not an active component of the device.

In comparing the Takashi et al. semiconductor device to Applicants' device, the Examiner is attempting to compare distinct levels of circuits. Takashi et al. provide a semiconductor device that may include a component 13. The component 13 is electrically connected to the P-type Si wafer substrate, as indicated by connection 21. Thus, the P-type Si wafer substrate 16, interconnect layer 17 and component 13 form an integral semiconductor device. Particularly, the capacitor 24 is formed as part of the interconnect layer 17. Applicants describe such devices and their shortcomings (page 4, lines 1-9).

Applicants, on the other hand, recite a device that can interconnect a plurality of semiconductor, or circuit, devices. The circuit devices 20 are not electrically connected to the support base 12. The decoupling capacitors are separate components and the interconnect layer is formed *over* the decoupling capacitors (Figs. 4-7). The decoupling capacitors are *mounted on* a surface, such as support base 12. A filler can be deposited between the components mounted on the surface to provide mechanical support (page 13, lines 16-20). The capacitors include a grounding pad and a power pad formed on a top surface of the decoupling capacitors, allowing for electrical connection to the pads of the decoupling capacitors. The interconnect layer 16 can then be *formed over* the decoupling capacitors.

Takashi et al. fail to disclose a *device for interconnecting a plurality of circuit devices having a decoupling capacitor mounted on a first surface* with *a grounding pad and a power pad formed on a top surface of the decoupling capacitor*; and *an interconnect layer having a pattern of circuit connections formed over the top surface of the decoupling capacitor*, whereby *electrical connections to the decoupling capacitor are embedded within the interconnect layer*